MODULAR REGISTER ARRAY

Abstract

An integrated circuit includes a register array having a number of entry groups. Each of the entry groups includes multiple entries. Each of the entries has multiple bits. The bits among different entries are grouped into bit groups. The integrated circuit also includes a number of output ports. Each of the output ports has multiple selecting units. Each of the selecting units connects to one of the bit groups. The integrated circuit further includes a number of match ports. Each of the match ports has multiple comparing units. Each of the comparing units connects to one of the bit groups.

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